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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,592	04/21/2004	Betty Shu Mercer	TI-36275	5550

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
08/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/828,592	MERCER ET AL.	
	Examiner	Art Unit	
	STEVEN J. FULK	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-16 and 18-22* is/are pending in the application.

4a) Of the above claim(s) *11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,16 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5, 6, 9, 10, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. '692 in view of Kondo '858, or in the alternative, as being unpatentable over by Lee et al. '692 in view of Bojkov et al. '048, and further in view of Kondo '858.

a. Regarding claims 1, 2, 4, 5, 6, 10, 16 and 20, Lee discloses a method for manufacturing an integrated circuit (figs. 7-14), comprising: forming transistor devices over a semiconductor substrate (fig. 7, substrate 10; ¶10, integrated circuits in substrate); forming one or more metallization layers over the transistor devices, the one or more metallization layers interconnecting one or more of the

transistor devices (¶12, integrated circuits connected to bond pad 32 though metal layers); forming a silicon nitride protective overcoat (34) over the one or more metallization layers, wherein the protective overcoat has an opening located therein; forming a surface conductive lead (fig. 9, 38) in the opening formed within the protective overcoat and over a TiW barrier layer (36), the barrier layer providing additional adhesion between the protective overcoat and the surface conductive lead (layers 34/36/38 are the same materials disclosed by the applicant, therefore the adhesion properties are the same as claimed), a portion of the barrier layer extending beyond the surface conductive lead (fig. 9); providing a seed layer (¶82) directly contacting the barrier layer and at least partially within the opening of the barrier layer; subjecting the portion of the barrier layer to an anisotropic etch to remove the portion and form a skirt (embodiment of figs. 14 & 16, ¶95, 97 & 107 ; anisotropic etch results in skirt extension of barrier layer past surface conductive lead), the anisotropic etch selective to the barrier layer (layer 36 is etched while underlying layers 34, 30, etc are not); and subjecting the seed layer to a wet etch prior to subjecting the portion of the barrier layer to the anisotropic etch, (¶94; fig. 12, partial etching of copper surface conductive lead 38 by wet etch would inherently remove the copper seed layer to expose barrier layer for subsequent etching in fig. 14), wherein the wet etch is without substantially undercutting the etched seed layer or surface conductive lead (figs. 6 & 12, width of surface conductive lead is reduced by 0.2um, which is interpreted as not "substantially" undercutting the

lead). See Erdos '071 for evidence that etching a surface lead and seed layer comprising the same material will result in removal of the seed layer and thinning of the surface conductive lead (Erdos, col. 4, lines 1-9), and the etch also exposes the barrier layer for subsequent etching.

While Lee discloses the barrier layer to be anisotropically etched, the reference does not explicitly teach the anisotropic etch to comprise a dry etch. Kondo discloses a method for manufacturing an integrated circuit (figs. 7A-7E), comprising forming a protective overcoat (104) over one or more metallization layers, wherein the protective overcoat has an opening located therein; forming a surface conductive lead (fig. 7D, 108) in the opening formed within the protective overcoat and over a barrier layer (105), a portion of the barrier layer extending beyond the surface conductive lead (fig. 7D); providing a seed layer directly contacting the barrier layer (seed layer 106/107 directly contacts barrier layer 105; Applicant's definition of a seed layer includes a multi-layer seed layer, Specification, Paragraph [0032]) and at least partially within the opening of the barrier layer; and subjecting the portion of the barrier layer to a dry etch comprising comprise carbon tetrafluoride and chlorine to remove the portion and form a skirt (fig. 7E; col. 10, lines 33-39; col. 7, lines 65-67, diameter of barrier layer is larger than surface lead), the dry etch selective to the barrier layer (layer 105 is etched while underlying layers 104, 101, etc are not).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the carbon tetrafluoride and chlorine dry etch

chemistry of Kondo in the method of Lee (or Lee in view of Bojkov). One would have been motivated to do this because Kondo taught that carbon tetrafluoride and chlorine dry etches were effective for removing TiW layers with a well controlled etch rate (col. 10, lines 33-39).

Alternatively, assuming *arguendo* that it was not inherent to remove the seed layer when partially etching the surface conductive lead, it would nonetheless have been obvious to one of ordinary skill in the art to remove the seed layer by wet etch. Bojkov teaches a method of manufacturing an interconnect comprising forming a surface conductive lead (fig. 4, 301) in an opening formed within a protective overcoat (102); the lead formed over seed layer (105a/105b); and subjecting the seed layer to a wet etch (¶34; Bojkov also teaches this etch will remove portions of the surface conductive lead 301, providing further evidence of the inherency argument above). Further evidence of obviousness of using a wet etch to remove the seed layer is provided by Applicant's Admitted Prior Art, stating that wet etching is a well known, effective method of removing the seed layer (Specification, page 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the seed layer by wet etch. One would have been motivated to do this because wet etching was a well known, conventional method of removing metal layers in semiconductor devices that provided the advantages of low cost and simple processing.

b. Regarding claims 9 and 19, Lee (or Lee in view of Bojkov) in view of Kondo discloses all of the elements of the claim(s) as set forth in paragraph 4a above, but the Lee does not explicitly disclose the surface conductive lead to have a width ranging from 3 to 200 μm. Kondo teaches a method of forming a surface conductive lead having a width ranging from 3 to 200 μm (col. 4, lines 20-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the surface conductive lead of Lee (or Lee in view of Bojkov) to the width as taught by Kondo. One would have been motivated to do this because Lee taught that the pitch of state-of-the-art surface conductive leads was approximately 200 μm, meaning the width of the lead itself would need to be less than 200 μm. The surface lead width of Kondo would also allow the fine pitch interconnect desired by Lee (Lee, paragraph 26) and allow high density integration of the circuits.

4. Claims 8 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. '692 in view of Kondo '858, and further in view of Bojkov et al. '048.

Lee (or Lee in view of Bojkov) in view of Kondo teaches all of the elements of the claims as set forth in paragraph 3a above, but Lee does not explicitly disclose the wet etch chemistry to include hydrogen peroxide and sulfuric acid. Bojkov teaches a method of etching the copper seed layer using a wet etch chemistry including hydrogen peroxide and sulfuric acid (¶34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the wet etch chemistry of Bojkov in the method for manufacturing an interconnect as described by Lee (or Lee in view of Bojkov) in view of Kondo. One would have been motivated to do this because Bojkov taught that a wet etch chemistry including hydrogen peroxide and sulfuric acid was a well known, convenient chemistry used to etch copper seed layers (¶34). Further evidence of obviousness of using a chemistry including hydrogen peroxide and sulfuric acid is provided by Backus '124, which taught that a wet etch chemistry including hydrogen peroxide and sulfuric acid (col. 2, lines 43-51) was a well known chemistry used to etch copper that also prevented cementation of copper onto other metal surfaces during etching (col. 1, lines 28-35), thus providing a clean surface conductive lead for subsequent wire-bonding and packaging steps.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee '692 in view of Kondo '858, and further in view of Ashby et al. '238; or in the alternative, as being unpatentable over by Lee et al. '692 in view of Bojkov et al. '048, further in view of Kondo '858, and further in view of Ashby et al. '238.

Lee (or Lee in view of Bojkov) in view of Kondo teaches all of the elements of the claims as set forth in paragraph 3a above, but the references do not explicitly teach the use of nitrous oxide in the dry etch chemistry. Ashby et al. teaches a method of etching tungsten titanium alloys (col. 4, lines 2-6) using a dry etch chemistry of carbon tetrafluoride and nitrous oxide, oxygen or chlorine (col. 4, lines 58-65; col. 6, lines 29-47) in the fabrication of integrated circuits (col. 4, lines 31-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dry etch chemistry of Ashby et al. in the method for manufacturing an interconnect of Lee (or Lee in view of Bojkov) in view of Kondo. One would have been motivated to do this because Kondo taught that it was desirable to use a conventional dry etch that included Cl_2, BCl_3,CF_4, or the like (col. 10, lines 35-39), and Ashby et al. taught that a dry etch chemistry of carbon tetrafluoride and nitrous oxide, oxygen or chlorine was well known to be highly selective to the tungsten titanium alloy, thus removing the barrier layer without damaging the surrounding layers of the device (Ashby et al., col. 2, lines 40-52).

9. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. '692 in view of Kondo '858, and further in view of Nye, III et al. '286, or in the alternative, as being unpatentable over by Lee et al. '692 in view of Bojkov et al. '048, further in view of Kondo and further in view of Nye, III et al. '286.

Lee (or Lee in view of Bojkov) in view of Kondo discloses all of the elements of the claim(s) as set forth in paragraph 3a above, including etching the barrier layer with a dry etch comprising carbon tetrafluoride to form a skirt, but the reference does not explicitly disclose the resulting skirt to taper down as it moves away from the surface conductive lead.

Nye teaches a method for manufacturing an interconnect for an integrated circuit, comprising forming transistor devices over a semiconductor substrate (fig. 4A, substrate 200); forming one or more metallization layers over the transistor devices, the one or more metallization layers interconnecting one or more of the transistor devices

(metallization 210); forming a protective overcoat (layer over 210) over the one or more metallization layers, wherein the protective overcoat has an opening (215) located therein; forming a surface conductive lead (300) in the opening formed within the protective overcoat and over a barrier layer (240), a portion of the barrier layer extending beyond the surface conductive lead (fig. 4A, layer 240 tapers out away from 300); providing a seed layer (260/280) directly contacting the barrier layer and at least partially within the opening of the barrier layer; subjecting the portion of the barrier layer to a dry etch comprising fluorocarbons to remove the portion and form a skirt that tapers down as it moves away from the surface conductive lead (fig. 4A; col. 6, lines 29-37 & 63-65), the dry etch selective to the barrier layer (fig. 4A, layers under 240 are not etched).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the tapered skirt of Nye in the method of Lee (or Lee in view of Bojkov) in view of Kondo. One would have been motivated to do this because Nye taught that the barrier layer edge should have a tapered profile in order to minimize stress induced cracks in the underlying insulators (Nye, col. 6, lines 33-37).

Response to Arguments

6. Applicant's arguments with respect to the rejection of claims 1, 2, 4-6, 9, 10, 16, 19 and 20 over Kondo '858 have been fully considered and are persuasive. The rejection of claims 1, 2, 4-6, 9, 10, 16, 19 and 20 over Kondo '858 has been withdrawn.

7. Applicant's arguments with respect to the rejection of claims 1 and 16 over Lee or Lee in view of Bojkov, wherein the Applicant argued that Lee does not specifically

disclose whether the anisotropic etch of the embodiment of figs. 14 & 16 is a dry etch, have been considered but are moot in view of the new grounds of rejection set forth above.

8. Applicant's arguments with respect to the rejection of claims 1 and 16 over Lee or Lee in view of Bojkov, wherein the Applicant argued the wet etch of Lee is intended to reduce the diameter of the surface conductive lead and this is equivalent to "substantially undercutting" the surface conductive lead, have been considered but are not found persuasive. The term "undercutting" is defined by the Applicant's Specification as reducing "the width of the conductive lead at its base" (Specification, ¶[0018]), which is known in the art to mean a reduction in the width at the base relative to the width of the top surface of the conductive lead. The etching step of Lee reduces the overall size of the surface conductive lead, not just the base of the lead. Therefore, no "undercut" is produced in the lead by the etching step of Lee.

Assuming *arguendo* that "undercutting" is defined as any reduction in the width of the base of the conductive lead, even if the reduction is of the entire lead at both the base and the top of the lead, the etching step of Lee is still not considered to be "substantially undercutting" the lead. Applicant's Specification defines an undercutting of 14 % to 30% reduction in width of the base to be acceptable, in that it "does not cause too many problems" (Specification, ¶[0018]). Lee discloses the reduction in width of the surface conductive lead to be 0.2μm (fig. 6). The width of the surface conductive lead as described by Lee in view of Kondo is 3 μm -200 μm (paragraph 3b above), which is a conventional width in the art. At the smallest width of 3 μm, a 0.2 μm

reduction would only be 6.67%. Because this is well below the acceptable range of 14-30% as defined by the Applicant, the wet etch of Lee is considered to not "substantially undercut" the surface conductive lead.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN J. FULK whose telephone number is (571)272-8323. The examiner can normally be reached on Monday through Friday, 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven J. Fulk
Patent Examiner
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August 11, 2008

/BRADLEY W BAUMEISTER/
Supervisory Patent Examiner, Art Unit 2891